REMARKS

Claims 1 and 3-23 are currently pending in the subject application and are presently under consideration. Claims 10 and 17 have been amended as shown at pages 2-5 of this reply. Favorable reconsideration of the subject patent application is respectfully requested in view of the comments and amendments herein.

I. Rejection of Claims 1, 3-8, 10 and 17-23 Under 35 U.S.C. §103(a)

Claims 1, 3-8, 10 and 17-23 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Singh, *et al.* (US 6,650,422 hereinafter referred to as Singh) in view of Singh, *et al.* (US 6,561,706 hereinafter referred to as Singh '706) and Arita (US 6,905,949). It is requested that this rejection be withdrawn for at least the following reasons. Singh, Singh '706, and Arita taken alone or in combination do not teach or suggest every element of the claimed invention, and one ordinarily skilled in the art could not combine these references to successfully implement the claimed invention, in fact they teach away from the claimed invention.

> To reject claims in an application under §103, an examiner must establish a *prima facie* case of obviousness. A *prima facie* case of obviousness is established by a showing of three basic criteria. First, there ***must be some suggestion or motivation***, either in the references themselves or in the knowledge generally available to ***one of ordinary skill in the art, to modify the reference or to combine reference teachings***. Second there must be a ***reasonable expectation of success***. Finally, the prior art reference (or references when combined) ***must teach or suggest all the claim limitations***. *See* MPEP §706.02(j). The ***teaching or suggestion to make the claimed combination*** and the reasonable expectation of success ***must be found in the prior art and not based on the Applicant's disclosure***. *See In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) (emphasis added).

The subject invention generally relates to a system capable of detecting and mitigating line-edge roughness in a semiconductor photoresist while maintaining specified critical dimensions. More specifically, independent claim 1, and similarly independent claims 10 and 17, recites a monitoring component that monitors information associated with at least one critical dimension and line-edge roughness on a photoresist, a non-lithographic shrink component that facilitates ***selectively mitigating*** line-edge roughness, and a trim etch component that facilitates

selectively satisfying the at least one critical dimension specification. As acknowledged by the Examiner in the Final Office Action dated April, 19, 2006, the references do not alone teach or suggest every element of the claimed invention. Also, even when taken in combination, the prior art references still fail to teach or suggest every element of the claimed invention.

The system in Singh is generally capable of deriving information from a fabricated semiconductor in order to improve the fabrication process for subsequent semiconductors. As contended by the Examiner, Singh adjusts *future* process parameters based on measured data of the pattern profiles. This is distinguishable from applicants' claimed invention in that the invention is concerned with mitigating line-edge roughness on an *ascertained* semiconductor. Also, the claimed invention is concerned with such mitigation regardless of which side of the semiconductor is affected. On the contrary, the asymmetry the Singh system aims to mitigate is that of one side of a semiconductor to the other. As a result, the Singh system rotates the device and compares the information of both sides to ascertain inconsistencies to be cured in subsequent fabrications. For this reason, the data collected, compared, and utilized between the monitoring components of the two systems is completely different such that the Singh system may disregard line-edge roughness if it were consistent on both sides.

Moreover, as disclosed in independent claims 1, 10, and 17, the subject invention is capable of ***selectively*** mitigating line-edge roughness on a given photoresist. According to the Examiner, Arita is depended upon to disclose mitigating line edge roughness. Arita generally relates to a system that smoothes edge roughness on the *entire* resist pattern of a given semiconductor. To this end, Arita, is a smoothing process for an ***entire*** photoresist pattern that requires an additional resin to be applied over the ***entire*** pattern where, after the edge roughness is corrected, the entire layer of resin is diluted and discarded. This system is wasteful of time and resources as compared to the subject invention that is capable of ***selectively*** smoothing only line-edges that do not meet the threshold for line-edge roughness specified in the monitoring component and not necessarily the entire pattern. For these reasons, the prior art systems, when taken alone or in combination, fail to teach or suggest every element of the claimed invention.

Additionally, because Singh relates to a system that profiles fabricated "test" semiconductors to gain information on how to improve certain steps in fabrication of subsequent semiconductors, and because Arita relates to a system that smoothes edge roughness on the *entire* resist pattern of a given semiconductor, combining these references would teach away

from the claimed invention. The system resulting from this combination would, at best, be capable of detecting edge-roughness in a "test" semiconductor and smoothing edges of *subsequent* semiconductors by smoothing *every* line in the pattern. This teaches away from the claimed invention in two ways. First, it dispenses with the advantageous ***selective*** functionality of the claimed invention whereby only lines that need smoothing are modified. Secondly, the combined invention is unable to cure a given semiconductor; only those *subsequently* fabricated may be cured as contrary to the subject invention.

Furthermore, due to the nature of the Arita system with the restriction that it be applied to the whole resist pattern, it is capable of a clean and accurate smoothing process over the entire pattern, which satisfies critical dimension specifications, and in turn, discards of the need for an etching process. Thus, the combination with the component of Singh '706 that is capable of achieving critical dimensions would be wholly unnecessary. This is not to say the etching process of the claimed invention is unnecessary, because the ***selective*** function of the claimed invention that distinguishes it from Arita, requires a ***selective*** etching process in order to efficiently satisfy the critical dimensions following the ***selective*** line-edge roughness smoothing process. For the foregoing reasons, one having ordinary skill in the art would have no motivation to combine the cited references as they teach away from the claimed invention (and to some extent teach away from each other), nor could they do so with a reasonable expectation of success.

Since combining the prior art systems could not be done with reasonable success without teaching away from the claimed invention, and since the references fail to teach or suggest every element of the claimed invention even if they could be combined, rejection of independent claims 1, 10, and 17 (as well as claims 3-8, 10 and 17-23 which respectively depend therefrom) should be withdrawn.

II. Rejection of Claims 9 and 11-16 Under 35 U.S.C. §103(a)

Claims 9 and 11-16 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Singh, *et al.* (US 6,650,422 hereinafter referred to as Singh) in view of Singh, *et al.* (US 6,561,706 hereinafter referred to as Singh '706) and Arita (US 6,905,949) as applied to claims 1-8, 10 and 17-23 above, and further in view of Kim, *et al.* (US 6,730,458 hereinafter referred to as

Kim). This rejection should be withdrawn for at least the following reasons. Claims 9, and 11-16 respectively depend from independent claims 1 and 10; and Kim fails to makeup for the aforementioned deficiencies rendered by Singh, Singh '706, and Arita with respect to the subject independent claims. Accordingly, withdrawal of this rejection is requested.

CONCLUSION

The present application is believed to be in condition for allowance in view of the above comments and amendments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063 [AMDP981US].

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicants' undersigned representative at the telephone number below.

Respectfully submitted,

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